REMARKS

Claims 1-17 are pending in the application. In the Office Action of September 4, 2002, the Examiner made the following disposition:

A.) Objected to the drawings.

B.) Objected to the Title of the Invention.

C.) Objected to the specification.

D.) Objected to claims 3, 14, 15, 16, 17.

E.) Rejected claims 11-15 under 35 U.S.C. §112, second paragraph.

F.) Rejected claims 14 and 15 under 35 U.S.C. §101.

G.) Rejected claims 1, 3-6, and 11-13 under 35 U.S.C. §102(e) as being anticipated by *Sauer*.

H.) Rejected claims 2 and 14-17 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Gowda*.

I.) Rejected claims 7 and 8 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Takemoto*.

J.) Rejected claims 9 and 10 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Tronnamuchai*.

Applicants respectfully traverse the rejections and address the Examiner's disposition below.

A.) Objection to the drawings:

Figure 1 has been labeled "RELATED ART" as per the Examiner's request to overcome the objection.

Regarding the term "Φm", page 15 of the specification has been amended to replace the term --Φm-- with "ΦVm". Accordingly, Applicants respectfully submit the drawings do not require amendment to include the term "Φm" as Figure 8 already includes the term "ΦVm".

Regarding the term "69", page 16 of the specification has been amended to replace the term --69-- with "59". Accordingly Applicants respectfully submit the drawings do not require amendment to include the term "69" as Figure 8 already includes the term "59".

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"VERSION WITH MARKING TO SHOW CHANGES MADE**. No new matter is added with the present amendments.

Applicants respectfully submit the objections have been overcome and request that they by withdrawn.

B.) Objection to the Title of the Invention:

The Title of the Invention has been amended as per the Examiner's request to overcome the objection. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"VERSION WITH MARKING TO SHOW CHANGES MADE**.

Applicant respectfully submits that the objection has been overcome and requests that it be withdrawn.

C.) Objection to the specification:

The specification has been amended as per the Examiner's request to overcome the objection.

Applicant respectfully submits that the objection has been overcome and requests that it be withdrawn.

D.) Objection to claims 3, 14, 15, 16, 17:

Claims 3, 14, 15, 16, and 17 have each been amended as per the Examiner's request to overcome the objections.

Applicants respectfully submit the objection has been overcome and request that it be withdrawn.

E.) Rejection of claims 11-15 under 35 U.S.C. §112, second paragraph:

Claims 11 and 14 have been amended as per the Examiner's request to overcome the rejection.

Claims 12, 13, and 15 depend directly or indirectly from claims 11 or 14 and are therefore allowable for at least the same reasons that claims 11 and 14 are allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

F.) Rejection of claims 14 and 15 under 35 U.S.C. §101:

Claim 14 has been amended as per the Examiner's request to overcome the rejection.

Claim 15 depends directly or indirectly from claim 14 and is therefore allowable for at least the same reasons that claim 14 is allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

G.) Rejection of claims 1, 3-6, and 11-13 under 35 U.S.C. §102(e) as being anticipated by *Sauer*:

Applicants respectfully disagree with the rejection.

Applicants' independent claim 1 has been amended to include the subject matter of claim 7. Accordingly, claim 7 has been cancelled. Claim 1, as amended, claims a selection switch and a read-out switch that each comprise a MOS transistor having a double gate structure.

Referring to Applicants' Figure 7 for illustrative purposes, as discussed in Applicants' specification, since Applicants' claimed switches comprise a MOS transistor having a double gate structure, neighboring portions of gate electrodes 13a and 14a of the selection MOS transistor 13 and the read-out MOS transistor 14 are overlapped with each other, so that an n+ diffusion region (as shown in Figure 4) does not occur between the gate electrodes 13a and 14a. Accordingly, a noise component due to a dispersion of a filed occurring in the read-out MOS transistor gate electrode 14a at the shift timing from the period d to the period e can be completely transferred. Therefore, there is not an occurrence of any noise due to the gate electrode 14a of the read-out MOS transistor 14. Further, the overflow charge from the photodiode 12 is supplied directly to the n+ diffusion region connected to the vertical signal line 15, so that smearing can be suppressed to the charges occurring within the one pixel read-out time by resetting the vertical signal line 15 just before the signal charge (pixel signal) is read out.

This is clearly unlike *Sauer*, which fails to disclose or even suggest a selection switch and a read-out switch that each comprise a MOS transistor having a double gate structure. As acknowledged by the Examiner on page 11 of the Office Action, *Sauer* fails to disclose transistors with a double-gate structure. Therefore, for at least this reason, *Sauer* fails to anticipate Applicants' claim 1.

Sauer in view of *Takemoto* also fails to disclose or suggest claim 1. *Takemoto* discloses gates 68 and 69 that overlap with each other, however, nowhere does *Takemoto* disclose or suggest gates that are formed within a pixel that overlap each other. As discussed above,

Applicants' selection transistor and read-out transistor beneficially have a double gate structure to transfer a noise component from the read-out transistor, as well as other benefits described above. Nowhere does *Sauer* or *Takemoto* even discuss transferring a noise component in such a manner. *Sauer* fails to teach using overlapping transistors in a pixel to transfer a noise component from the pixel, and *Takemoto* fails to teach that its gates can be used in a pixel or to transfer a noise component. In other words, unlike Applicants' claim 1, *Takemoto* merely discloses overlapped transistors, but does not teach a motivation to use its transistor in a pixel to transfer a noise component. Further, *Sauer* does not teach a motivation to use overlapped transistors in a pixel to transfer a noise component.

Therefore, *Sauer* in view of *Takemoto* still fails to disclose or suggest Applicants' claim 1.

Claims 3-6 and 11-13 depend directly or indirectly from claim 1 and are therefore allowable for at least the same reasons that claim 1 is allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

H.) Rejection of claims 2 and 14-17 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Gowda*:

Applicants respectfully disagree with the rejection.

Similar to claim 1, Applicants' independent claim 14 has been amended to include the subject matter of claim 7. Claim 14, as amended, claims a selection switch and a read-out switch that each comprise a MOS transistor having a double gate structure.

Therefore, similar to claim 1, claim 14 is allowable over *Sauer* for at least the reasons discussed above. *Gowda* still fails to disclose or suggest a selection switch and a read-out switch that each comprise a MOS transistor having a double gate structure. Therefore, *Sauer* in view of *Gowda* still fails to disclose or suggest claims 1 and 14.

Claims 2 and 15-17 depend directly or indirectly from claims 1 or 14 and are therefore allowable for at least the same reasons that claims 1 and 14 are allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

I.) Rejection of claims 7 and 8 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Takemoto*:

Applicants respectfully disagree with the rejection.

Claim 7 has been cancelled.

Claim 1 is allowable over *Sauer* in view of *Takemoto* as discussed above.

Claim 8 depends directly or indirectly from claim 1 and is therefore allowable for at least the same reasons that claim 1 is allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

J.) Rejection of claims 9 and 10 under 35 U.S.C. §103(a) as being unpatentable over *Sauer* in view of *Tronnamuchai*:

Applicants respectfully disagree with the rejection.

Claim 1 is allowable over *Sauer* as discussed above. *Tronnamuchai* still fails to disclose or suggest a selection switch and a read-out switch that each comprise a MOS transistor having a double gate structure. Therefore, *Sauer* in view of *Tronnamuchai* still fails to disclose or suggest claim 1.

Claims 9 and 10 depend directly or indirectly from claim 1 and are therefore allowable for at least the same reasons that claim 1 is allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-6 and 8-17 are patentable. It is therefore submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Drawings:

Please amend Figure 1 and as shown on the drawing sheet marked in red attached to the Request for Approval of Drawing Changes submitted herewith.

In the Specification:

Please replace the Title of the Invention with the following replacement Title of the Invention:

--SOLID-STATE IMAGE PICKUP DEVICE HAVING AN AMPLIFIER FOR EACH VERTICAL SIGNAL LINE AND DRIVING METHOD THEREFOR--

Please replace the paragraph beginning at page 3, line 17, with the following replacement paragraph:

--In each [of the] unit pixel of the solid-state image pickup device thus constructed, [each unit pixel has] there are a selection switch and a read-out switch[, so that]. Accordingly, the pixel signal can be read out for every pixel. Therefore, the vertical signal line is first reset, and then each pixel signal is read out to the vertical signal line, whereby the reset level and the signal level are obtained in this order pixel by pixel. Further, by calculating the difference between the reset level and the signal level, the noise component due to the dispersion of the pixel characteristic can be cancelled. In addition, the reset level and the signal level are output through the same route, so that any stripe-shaped noise component having correlation in the vertical direction does not occur in principle.--

Please replace the paragraph beginning at page 13, line 17, with the following replacement paragraph:

--As described above, the neighboring portions of the gate electrodes 13a, 14a of the selection MOS transistor 13 and the read-out MOS transistor 14 are overlapped with each other, whereby the n^+ diffusion region shown in Fig. 4 does not occur between the gate electrodes 13a, 14a, so that the noise component due to the dispersion of the field [through] occurring in the gate electrode 14a of the read-out MOS transistor 14 at the shift timing from the period d to the period e can be also completely transferred.--

Please replace the paragraph beginning at page 15, line 11, with the following replacement paragraph:

--Further, a vertical scan circuit 63 for line selection and a horizontal scan circuit 64 for column selection are provided. Each of these scan circuits 63 and 64 comprises a shift register, for example. The vertical scan pulse [Φm] ΦVm output from the vertical scan circuit 63 is applied to the vertical selection line 56, the read-out pulse ΦCn output from the horizontal scan circuit 64 is applied to the read-out pulse line 57, a horizontal scan pulse ΦHn is applied to the gate electrode of the horizontal selection MOS transistor 60, and a reset pulse ΦRn is applied to the gate electrode of the reset MOS transistor 62. A CDS circuit 66 having the circuit construction shown in Fig. 5 is provided as a differential circuit through a horizontal output amplifier 65.--

Please replace the paragraph beginning at page 16, line 12, with the following replacement paragraph:

--Subsequently, when the vertical scan pulse ΦVm is shifted to "H" level, the selection MOS transistor 53 of the unit pixel 51 of m-th line is turned on. When the reset pulse ΦRn is set to "H" level in this state, the reset MOS transistor 62 is turned on, and the vertical signal line 55 of n-th column is reset to the reference potential Vb of the column amplifier [69] 59. Thereafter, when the reset pulse ΦRn is shifted to "L" level and at the same time the horizontal scan pulse ΦHn is set to "H" level, the horizontal selection MOS transistor 60 is turned on, and the noise component is first output to the horizontal signal line 58 (period b).--

In the claims:

Please amend claims 1, 3, 11, 14, 15, 16, and 17 as follows:

1. (Amended) A solid-state image pickup device, [including] comprising:

a pixel portion having unit pixels arranged two-dimensionally in a matrix form, each of said unit pixels including a photoelectrically transducing element for photoelectrically transducing incident light to obtain a signal charge, and stocking the signal charge thus obtained, a selection switch for selecting [a pixel] one of the pixels, and a read-out switch for reading out the signal charge from said photoelectrically transducing element to [a] one of a plurality of vertical signal [line] lines;

[plural] a plurality of amplifying means, at least one of the amplifying means being [which are] connected to each of said respective vertical signal lines and [convert] for converting the signal charge read out to the vertical signal lines to an electrical signal; and

[plural] a plurality of reset means for resetting each of said vertical signal lines;

wherein each of said selection switch and said read-out switch comprises a MOS transistor having a double gate structure.

3. (Amended) The solid-state image pickup device as claimed in claim 1, wherein each of said reset means resets the respective vertical signal line in synchronism with a read-out timing before one pixel is read or a horizontal scan timing begins.

11. (Amended) The solid-state image pickup device as claimed in claim 1, wherein a horizontal selection switch for commonly outputting a reset level on said vertical signal line at a reset time of said reset means and a signal level read out onto said vertical signal line after the reset is provided between said vertical signal line and [said] a horizontal signal line.

14. (Amended) A method of driving a solid-state image pickup device[, characterized in that in a solid-state image pickup device including] comprising a pixel portion having unit pixels arranged two-dimensionally in a matrix form, each of said unit [pixel] pixels including a photoelectrically transducing element for photoelectrically transducing incident light to obtain a signal charge and stocking the signal charge thus obtained, a selection switch for selecting [a pixel] one of the pixels, and a read-out switch for reading out the signal charge from said photoelectrically transducing element to [a] one of a plurality of vertical signal [line] lines; [plural] a plurality of amplifying means at least one of which are connected to each of said respective vertical signal lines and [convert] for converting the signal charge read out to the vertical signal lines to an electrical signal[;], and a plurality of reset means for resetting each of said vertical signal lines, the method comprising the steps of:

resetting the vertical signal line [is first reset]; [and then]

after resetting the vertical signal line, reading out a pixel signal [is read out] from said photoelectrically transducing element to the vertical signal line to successively output [the] a reset level and [the] a signal level in this order through the same route[,]; and

[thereafter the] after reading out the pixel signal, calculating a difference between the reset level and the signal level [is calculated], wherein each of said selection switch and said read-out switch comprises a MOS transistor having a double gate structure.

15. (Amended) The solid-state image pickup device driving method as claimed in claim 14, wherein the solid-state image pickup device comprises a plurality of vertical selection lines, and wherein neighboring vertical selection lines are simultaneously driven two by two in turn, and signal charges of two pixels in [the] a vertical direction are mixed with each other on the vertical signal line.

16. (Amended) A camera [including] comprising:

an optical system for focusing incident light from a subject onto a solid-state image pickup device;

a driving system for driving said solid-state image pickup device; and

a signal processing system for processing an output signal of said solid-state image pickup device, wherein said solid-state image pickup device[,] comprises a pixel portion having unit pixels arranged [two-dimentionally] two-dimensionally in a matrix form, each of said unit pixels including a photoelectrically transducing element for photoelectrically transducing incident light to obtain signal charge, and stocking the signal charge thus obtained, a selection switch for selecting [a pixel] one of the pixels, and a read-out switch for reading out the signal charge from said photoelectrically transducing element to [a] one of a plurality of vertical signal [line] lines, [and] a plurality of [plural amplifying] means, at least one of which are connected to each of said respective vertical signal lines and [convert] for converting the signal charge read out to the vertical signal lines to an electrical signal, and a plurality of reset means for resetting each of said vertical signal lines, and wherein said driving system drives said solid-state image pickup device so that [the] one of the vertical signal [line] lines is first reset and then a pixel signal is read out from said photoelectrically transducing element to the vertical signal line to successively output [the] a reset level and [the] a signal level in this order through the same route, and thereafter calculates [the] a difference between the reset level and the signal level, and wherein each of said selection switch and said read-out switch comprises a MOS transistor having a double gate structure.

17. (Amended) The camera as claimed in claim 16, wherein the solid-state image pickup device comprises a plurality of vertical selection lines, and wherein neighboring vertical selection lines of said solid-state image pickup device are simultaneously driven two by two in turn, and signal charges of two pixels in [the] a vertical direction are mixed with each other on the vertical signal line to perform an interlace-supporting feedback read-out operation.

Please cancel claim 7.